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FQD2N60C / FQU2N60C

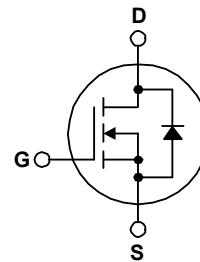
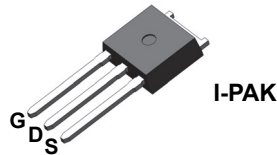
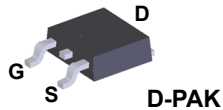
N-Channel QFET® MOSFET 600 V, 1.9 A, 4.7 Ω

Features

- 1.9 A, 600 V, $R_{DS(on)} = 4.7 \Omega$ (Max.) @ $V_{GS} = 10 V$, $I_D = 0.95 A$
- Low Gate Charge (Typ. 8.5 nC)
- Low Crss (Typ. 4.3 pF)
- 100% Avalanche Tested
- RoHS Compliant

Description

This N-Channel enhancement mode power MOSFET is produced using ON Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.



Absolute Maximum Ratings $T_C = 25^\circ C$ unless otherwise noted.

| Symbol | Parameter | FQD2N60CTM / FQU2N60CTU | Unit |
|----------------|---|-------------------------|---------------|
| V_{DSS} | Drain-Source Voltage | 600 | V |
| I_D | Drain Current - Continuous ($T_C = 25^\circ C$) | 1.9 | A |
| | Drain Current - Continuous ($T_C = 100^\circ C$) | 1.14 | A |
| I_{DM} | Drain Current - Pulsed (Note 1) | 7.6 | A |
| V_{GSS} | Gate-Source Voltage | ± 30 | V |
| E_{AS} | Single Pulsed Avalanche Energy (Note 2) | 120 | mJ |
| I_{AR} | Avalanche Current (Note 1) | 1.9 | A |
| E_{AR} | Repetitive Avalanche Energy (Note 1) | 4.4 | mJ |
| dv/dt | Peak Diode Recovery dv/dt (Note 3) | 4.5 | V/ns |
| P_D | Power Dissipation ($T_A = 25^\circ C$)* | 2.5 | W |
| | Power Dissipation ($T_C = 25^\circ C$) | 44 | W |
| | - Derate above $25^\circ C$ | 0.35 | W/ $^\circ C$ |
| T_J, T_{STG} | Operating and Storage Temperature Range | -55 to +150 | $^\circ C$ |
| T_L | Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds | 300 | $^\circ C$ |

Thermal Characteristics

| Symbol | Parameter | FQD2N60CTM / FQU2N60CTU | Unit |
|-----------------|--|-------------------------|--------------|
| $R_{\theta JC}$ | Thermal Resistance, Junction-to-Case, Max. | 2.87 | $^\circ C/W$ |
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient (minimum pad of 2 oz copper), Max. | 110 | |
| | Thermal Resistance, Junction-to-Ambient (* 1 in ² pad of 2 oz copper), Max. | 50 | |

Package Marking and Ordering Information

| Device Marking | Device | Package | Reel Size | Tape Width | Quantity |
|----------------|------------|---------|-----------|------------|------------|
| FQD2N60C | FQD2N60CTM | D-PAK | 330 mm | 16 mm | 2500 units |
| FQU2N60C | FQU2N60CTU | I-PAK | Tube | N/A | 70 units |

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted.

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|--|----------|-----|---------|--------------------------------|
| Off Characteristics | | | | | | |
| BV_{DSS} | Drain-Source Breakdown Voltage | $V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$ | 600 | -- | -- | V |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D = 250\ \mu\text{A}$, Referenced to 25°C | -- | 0.6 | -- | $\text{V}/^\circ\text{C}$ |
| I_{DSS} | Zero Gate Voltage Drain Current | $V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}$ $V_{DS} = 480\text{ V}, T_C = 125^\circ\text{C}$ | -- | -- | 1 10 | μA μA |
| I_{GSSF} | Gate-Body Leakage Current, Forward | $V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$ | -- | -- | 100 | nA |
| I_{GSSR} | Gate-Body Leakage Current, Reverse | $V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$ | -- | -- | -100 | nA |
| On Characteristics | | | | | | |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$ | 2.0 | -- | 4.0 | V |
| $R_{DS(on)}$ | Static Drain-Source On-Resistance | $V_{GS} = 10\text{ V}, I_D = 0.95\text{ A}$ | -- | 3.6 | 4.7 | Ω |
| g_{FS} | Forward Transconductance | $V_{DS} = 40\text{ V}, I_D = 0.95\text{ A}$ | -- | 5.0 | -- | S |
| Dynamic Characteristics | | | | | | |
| C_{iss} | Input Capacitance | $V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$ | -- | 180 | 235 | pF |
| C_{oss} | Output Capacitance | | -- | 20 | 25 | pF |
| C_{riss} | Reverse Transfer Capacitance | | -- | 4.3 | 5.6 | pF |
| Switching Characteristics | | | | | | |
| $t_{d(on)}$ | Turn-On Delay Time | $V_{DD} = 300\text{ V}, I_D = 2\text{ A},$ $R_G = 25\ \Omega$ | -- | 9 | 28 | ns |
| t_r | Turn-On Rise Time | | -- | 25 | 60 | ns |
| $t_{d(off)}$ | Turn-Off Delay Time | | -- | 24 | 58 | ns |
| t_f | Turn-Off Fall Time | | (Note 4) | -- | 28 | 66 |
| Q_g | Total Gate Charge | $V_{DS} = 480\text{ V}, I_D = 2\text{ A},$ $V_{GS} = 10\text{ V}$ | -- | 8.5 | 12 | nC |
| Q_{gs} | Gate-Source Charge | | -- | 1.3 | -- | nC |
| Q_{gd} | Gate-Drain Charge | | (Note 4) | -- | 4.1 | -- |
| Drain-Source Diode Characteristics and Maximum Ratings | | | | | | |
| I_S | Maximum Continuous Drain-Source Diode Forward Current | | -- | -- | 1.9 | A |
| I_{SM} | Maximum Pulsed Drain-Source Diode Forward Current | | -- | -- | 7.6 | A |
| V_{SD} | Drain-Source Diode Forward Voltage | $V_{GS} = 0\text{ V}, I_S = 1.9\text{ A}$ | -- | -- | 1.4 | V |
| t_{rr} | Reverse Recovery Time | $V_{GS} = 0\text{ V}, I_S = 2\text{ A},$ $di_F / dt = 100\text{ A}/\mu\text{s}$ | -- | 230 | -- | ns |
| Q_{rr} | Reverse Recovery Charge | | -- | 1.0 | -- | μC |

NOTES:

1. Repetitive Rating : Pulse width limited by maximum junction temperature.
2. $L = 56\text{ mH}, I_{AS} = 2\text{ A}, V_{DD} = 50\text{ V}, R_G = 25\ \Omega$, starting $T_J = 25^\circ\text{C}$.
3. $I_{SD} \leq 2\text{ A}, di/dt \leq 200\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$, starting $T_J = 25^\circ\text{C}$.
4. Essentially independent of operating temperature.

Typical Performance Characteristics

Figure 1. On-Region Characteristics

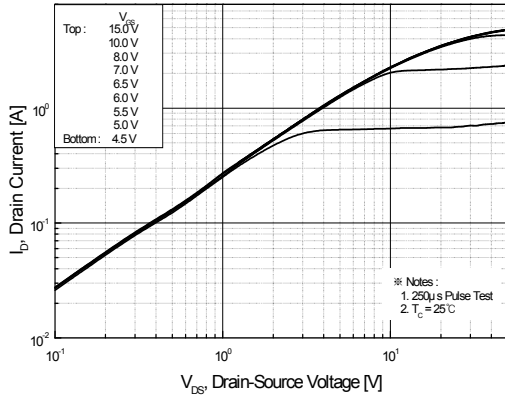


Figure 2. Transfer Characteristics

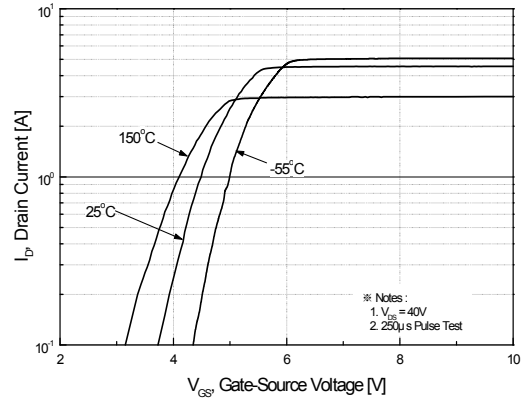


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

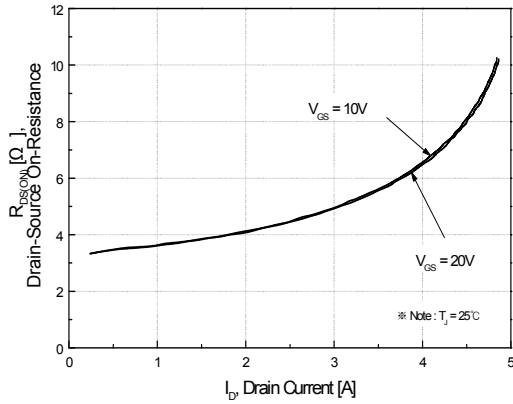


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

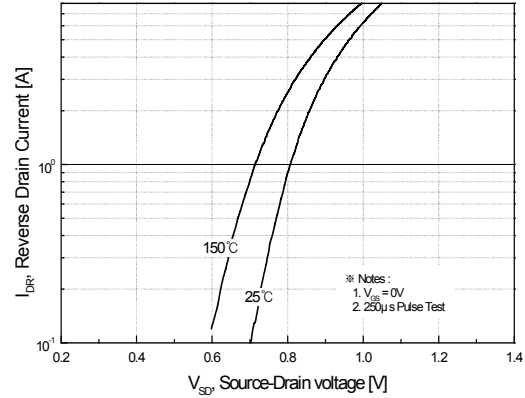


Figure 5. Capacitance Characteristics

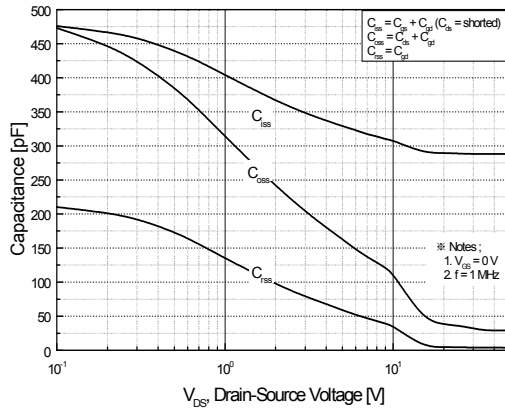
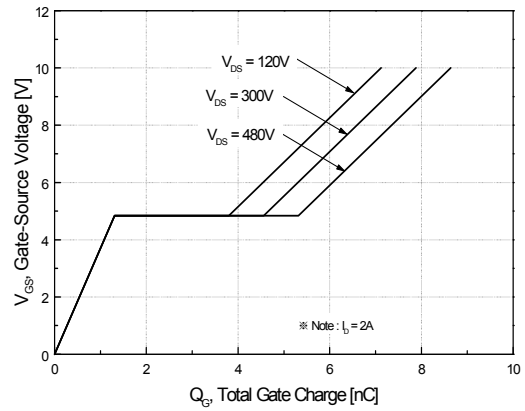


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

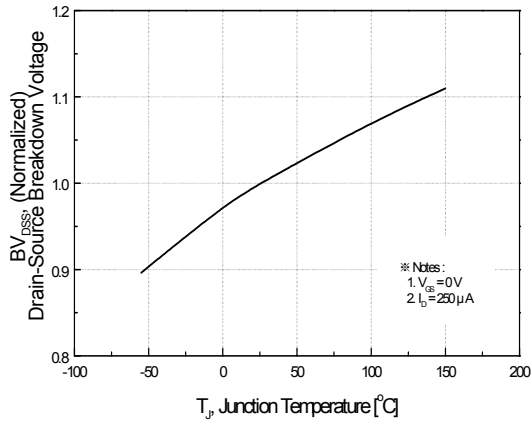


Figure 8. On-Resistance Variation vs. Temperature

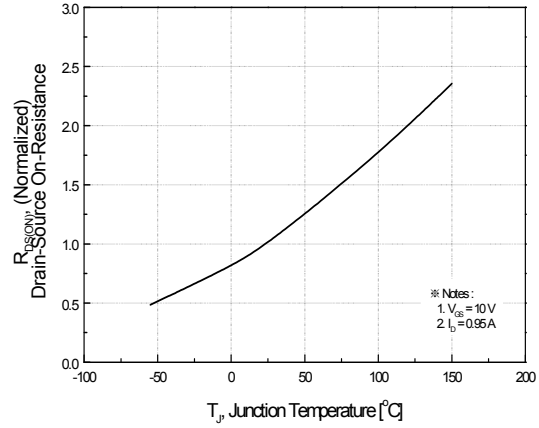


Figure 9. Maximum Safe Operating Area

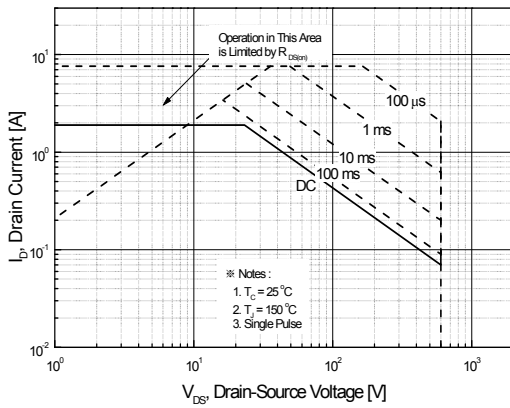


Figure 10. Maximum Drain Current vs. Case Temperature

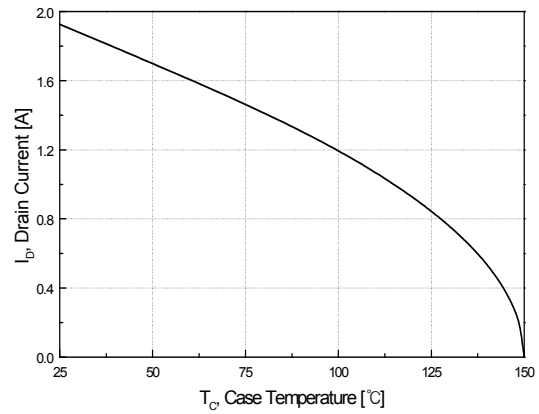


Figure 11. Transient Thermal Response Curve

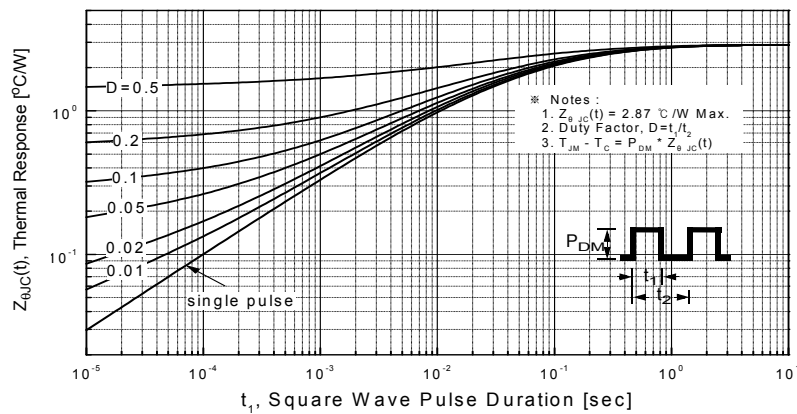


Figure 12. Gate Charge Test Circuit & Waveform

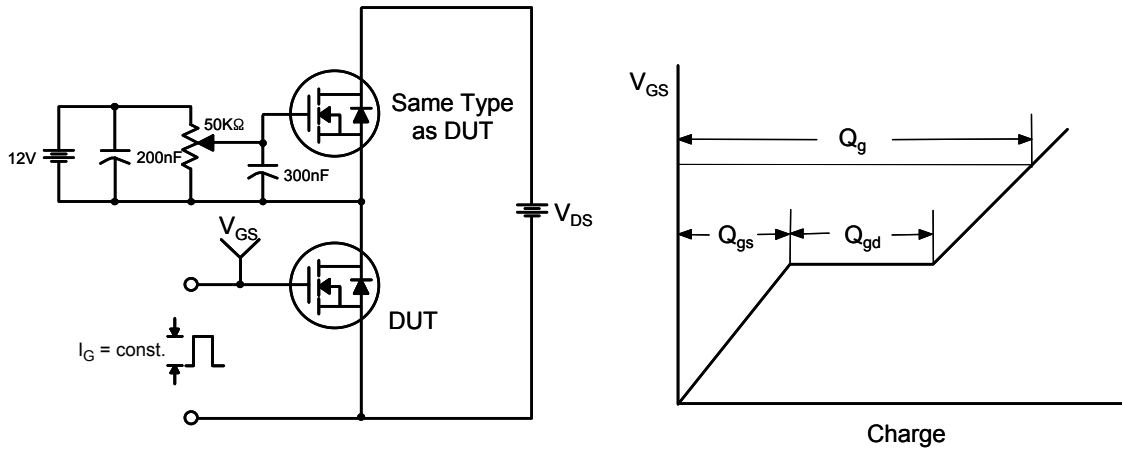


Figure 13. Resistive Switching Test Circuit & Waveforms

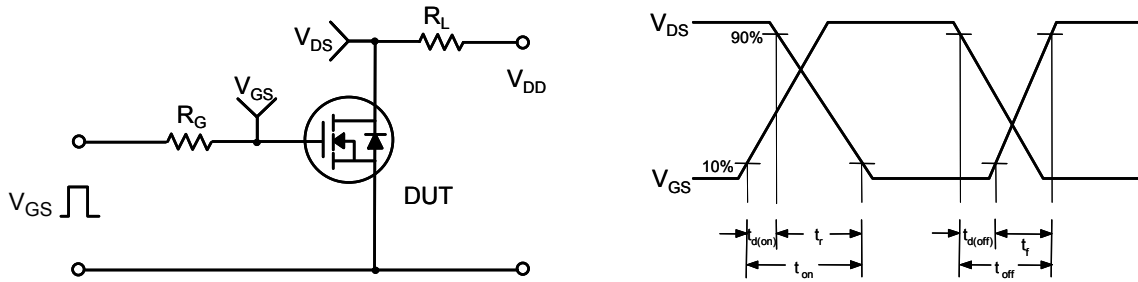


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

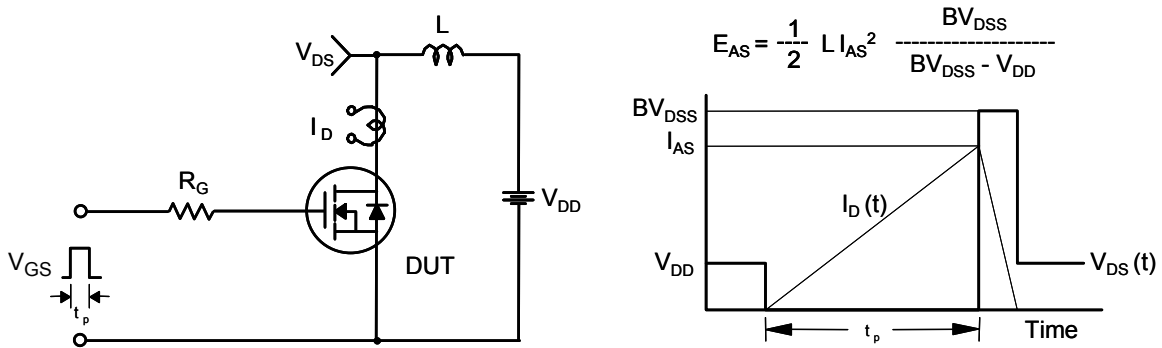
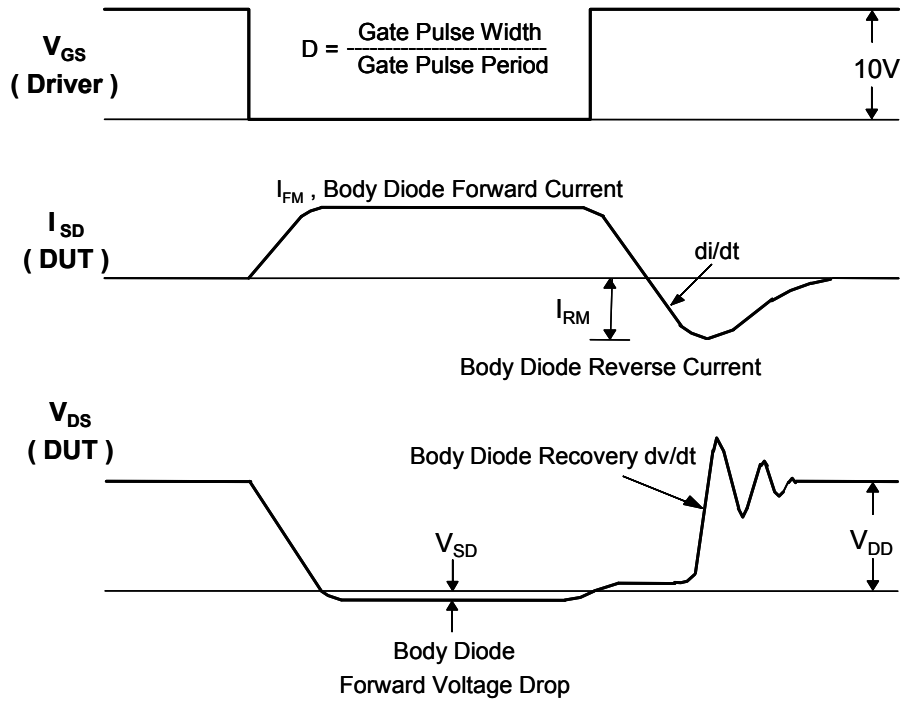
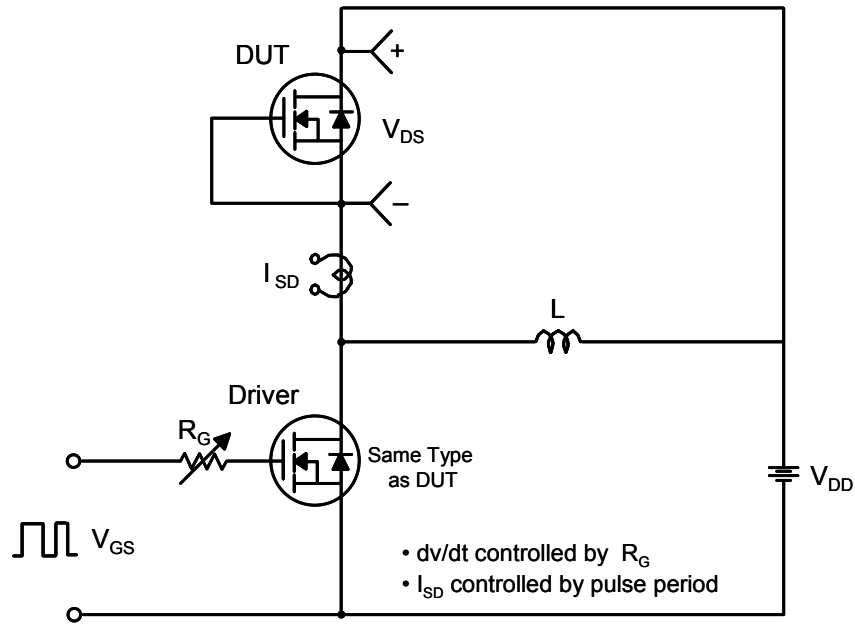


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms



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