

Datasheet

Sterling[™]-EWB

Version 1.9

REVISION HISTORY

Version	Date	Notes	Contributor(s)	Approver
1.0	26 June 2019	Initial version	Dave Neperud, Aaron Arbiture	Jay White
1.1	24 July 2019	Updated Regulatory section with new certifications; [™] added to required module names.	Maggie Teng	Jay White
1.2	05 Aug 2019	Updated Bluetooth SIG section	Jonathan Kaye	Jay White
1.3	28 Aug 2019	Corrected the Pin 80 VBAT description	Dave Neperud	Jay White
1.4	26 Feb 2020	Corrected Pin 21 description in Table 1	Dave Neperud	Jay White
1.5	28 Aug 2020	Updated Bluetooth certification to Bluetooth 5.1 (Errata) BR DR/LE	Bob Monroe	Jay White
1.6	09 Dec 2020	Updated all regulatory information	Ryan Urness	Jonathan Kaye
1.7	14 Jan 2021	Moved regulatory information to separate document	Sue White	Jonathan Kaye
1.8	15 Mar 2021	Added information about regulatory testing	Bob Monroe	Jonathan Kaye
1.9	15 July 2021	Removed Pending for Certifications	Dave Drogowski	Rick Tretow

CONTENTS

1	Scope	4
2	Introduction	4
3	Module Variants	5
4	Ordering Information	6
5	Block Diagram.....	8
6	Base SiP Module Footprint and Pin Definitions.....	9
7	U.FL/Chip Antenna Module Footprint and Pin Definitions.....	15
8	Specifications.....	19
8.1	General Characteristics	19
8.2	Power Supply Requirements.....	19
8.3	Maximum Ratings.....	20
8.4	WLAN Power Consumption	20
8.5	Bluetooth Power Consumption.....	20
8.6	WLAN RF Characteristics	21
8.7	Bluetooth RF Characteristics.....	23
9	MCU Interface Characteristics	24
9.1	DC Characteristics – General Input and Output	24
9.2	I2C Interface	25
9.3	SPI Interface	26
10	MCU UART Interfaces.....	27
10.1	Overview.....	27
10.2	Soldering Recommendations	27
10.3	Recommended Reflow Profile for Lead Free Solder.....	27
11	Wi-Fi MAC IDs/Bluetooth MAC IDs	28
12	Mechanical Details	28
13	Cleaning	34
14	Optical Inspection.....	34
15	Rework	34
16	Shipping, Handling, and Storage.....	35
17	Regulatory	36
18	Bluetooth SIG Qualification.....	36

1 SCOPE

This document describes key hardware aspects of the Laird Connectivity Sterling™-EWB.

2 INTRODUCTION

2.1 General Description

The Laird Connectivity Sterling™-EWB is a high performance 2.4 GHz WLAN and Bluetooth combo module based on latest-generation silicon (Cypress's CYW4343W) with an integrated ST Micro STM32F412 Cortex M4 MCU. With an industrial temperature rating, broad country certifications, and the availability of three different package styles, the Sterling-EWB provides significant flexibility to meet various end user application needs.

The on-module chip antenna package style for the Sterling-EWB eliminates complexity for design integration, simplifies manufacturing assembly with larger pin outs, and features an advanced chip antenna that offers greater resistance to de-tuning than typical trace or chip antennas.



2.2 Features Summary

- IEEE 802.11 b/g/n (single stream n)
- Bluetooth 5.1 (Errata) BR DR/LE
- Cortex M4 microprocessor
- Typical WLAN transmit power:
 - +17.5 dBm, 11 Mbps, CCK (b)
 - +14.0 dBm, 54 Mbps, OFDM (g)
 - +12.5 dBm, HT20 MCS7 (n)
- Typical WLAN sensitivity:
 - -88 dBm, 8% PER, 11 Mbps (b)
 - -75 dBm, 10% PER, 54 Mbps (g)
 - -72 dBm, 10% PER, MCS7 (n)
- WLAN and Bluetooth coexistence
- Available in two footprint styles:
 - Easy to Integrate: 16 mm x 21 mm
 - Miniature footprint: 10 mm x 10 mm
- Available with integrated chip antenna or U.FL connector for external antenna
- Operating voltage: 3.0V to 3.6V
- Operating temperature: -40° to +85° C
- Storage temperature: -40° to +125° C
- Compact design based on Cypress CYW4343W SoC and STM32F412 MCU
- Worldwide acceptance: FCC (USA), IC (Canada), ETSI (Europe), MIC (Japan), and RCM (AU/NZ)
- BT SIG QDID: D043845
- REACH and RoHS-compliant

WLAN

- IEEE 802.11b/g/n 1x1 2.4 GHz radio
 - Internal power amplifier (PA)
 - Internal low noise amplifier (LNA)
 - Internal T/R switch
 - Simultaneous BT/WLAN reception with a single antenna.
- Media Access Controller (MAC)
- Physical Layer (PHY)
- Baseband processor
- Standards
 - IEEE 802.11b, 802.11g, 802.11n (single stream)

Bluetooth

- Class 1 power amplifier with Class 2 capability
- HCI interface using high speed UART
- PCM for audio data
- Bluetooth 5.1 (Errata) BR DR/LE

Microcontroller

- STM32 Arm 32-bit Cortex™-M4 with a frequency up to 100 MHz
- 1 MB internal flash
- 256 kB of SRAM
- 2 MB SPI flash
- SPI, QSPI, USART, PCM
- ADC, I2C, I2S, GPIO, Timers
- JTAG
- WICED Fully compatible

Wireless Security System Features – Supported Modes in WICED

- Open (no security)
- WEP
- WPA Personal
- WPA2 Personal
- WMM
- WMM-PS (U-APSD)
- WMM-SA
- WAPI
- AES (Hardware accelerator)
- TKIP (host-computed)
- CKIP (SW support)

2.3 Applications

- Security and building automation
- Internet of Things/M2M connectivity
- Smart gateways

3 MODULE VARIANTS

The Laird Connectivity Sterling-EWB module is available in three different versions. Depending on your antenna and footprint needs, there is a variant to suit most application requirements. We recommend, for simplicity of both the host PCB design and the manufacturing process, that you use either the chip antenna or RF connector version of the modules.

- **453-00012 - Base SiP Module**

This module variant is supplied in a compact, 151 pin, 0.5 mm pitch LGA footprint. Unlike the other module variants, it requires the addition of either an off-module antenna or RF connector, as well as the associated matching components. To benefit from the EMC certifications on the module, you must strictly follow the layout in the module application guide. This requires adherence to the PCB stack-up and layout around the antenna. The footprint of this module may require additional care during reflow and PCB assembly.



Figure 1 Sterling-EWB Base SiP module (453-00012)

- **453-00013 – U.FL Module**

This module variant integrates the 450-00012 base SiP module, a U.FL RF connector, and all associated RF matching components on a PCB. This integrated approach not only provides a U.FL connector for connections to external antennas, but also simplifies and reduces the cost of the end users host board by simplifying the module PCB footprint.



Figure 2: Sterling-EWB U.FL module (453-00013)

- **453-00014 - Chip Antenna Module**

This module variant integrates the 453-00012 base SiP module, a chip antenna, and all associated RF matching components on a PCB. This integrated approach not only provides an external antenna solution, but also simplifies and reduces the cost of the end users host board by simplifying the module PCB footprint.






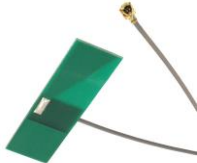


Figure 3 Sterling-EWB chip antenna module (453-00014)

4 ORDERING INFORMATION

Part Number	Description
453-00013C	Sterling-EWB U.FL module (Cut Tape)
453-00013R	Sterling-EWB U.FL module (Tape and Reel, SPQ = 1000)
453-00014C	Sterling-EWB chip antenna module (Cut Tape)
453-00014R	Sterling-EWB chip antenna module (Tape and Reel, SPQ = 1000)
453-00012C	Sterling-EWB base SiP module (Cut Tape)
453-00012R	Sterling-EWB base SiP module (Tape and Reel, SPQ = 2000)
455-00030	Sterling-EWB development kit, Chip Antenna
455-00031	Sterling-EWB development kit, FlexPIFA Antenna

4.1 Module Accessories

Part Number	Description	Image
001-0001	2.4 GHz dipole antenna with reverse polarity SMA connector	
080-0001	U.FL to reverse polarity SMA bulkhead cable 105 mm	
001-0014	2.4 GHz FlexPIFA antenna	
001-0015	2.4 GHz FlexNotch antenna	
001-0030	2.4 GHz Metal FlexPIFA antenna w/U.FL cable, 100 mm	
MAF94045	2.4 GHz NanoBlue Antenna	

5 BLOCK DIAGRAM

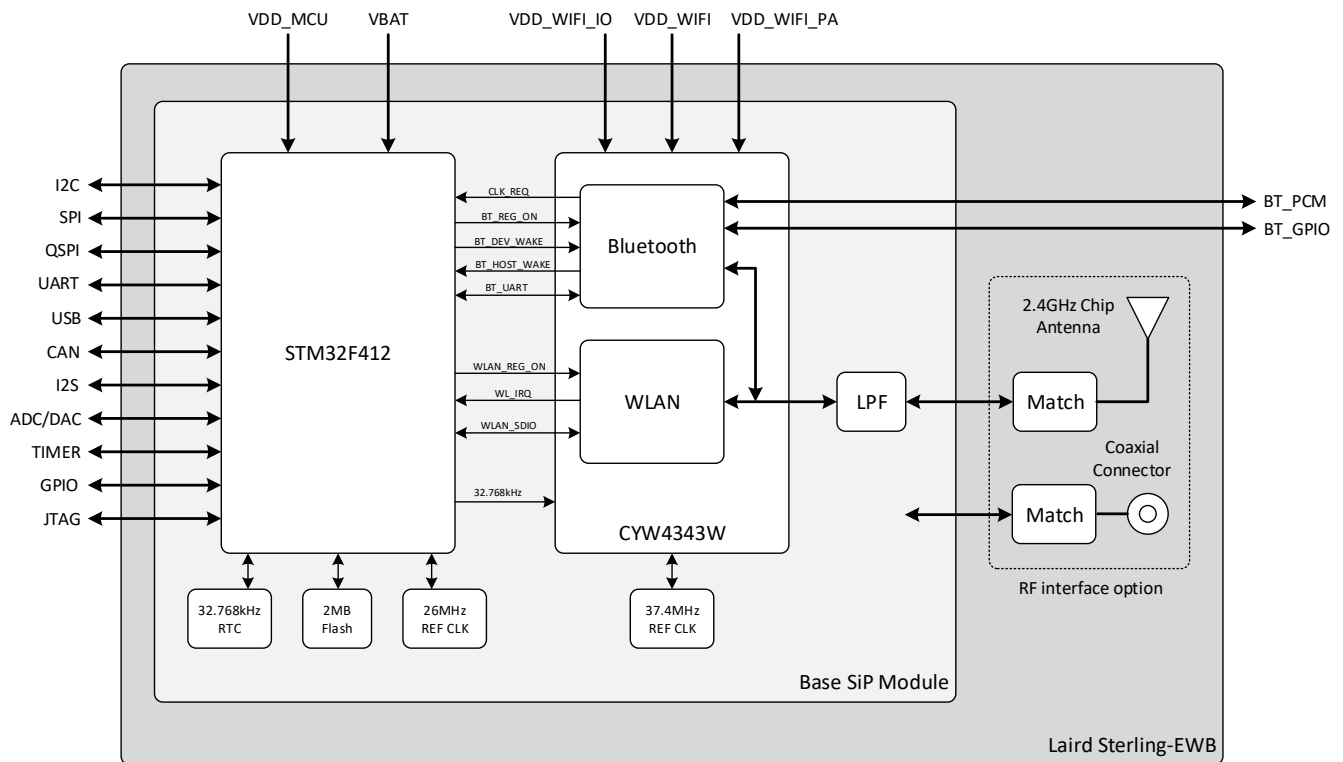


Figure 4: Sterling-EWB U.FL/chip antenna module block diagram

6 BASE SiP MODULE FOOTPRINT AND PIN DEFINITIONS

Note: The following footprint and pin definitions apply to the Sterling-EWB base SiP module (453-00012). There are two module footprints, depending on which variant of the module is used. *It is important to ensure you are using the correct version on your design.*

Note on regulatory testing:

It is important that you provide a JTAG interface (same as the DEBUG PROGRAM on the development kit) in your design so that you can load the required regulatory testing software on to your device via the WICED SDK. Please see the EWB Certification Instructions for information on setting up the testing.

6.1 Base SiP Module Footprint

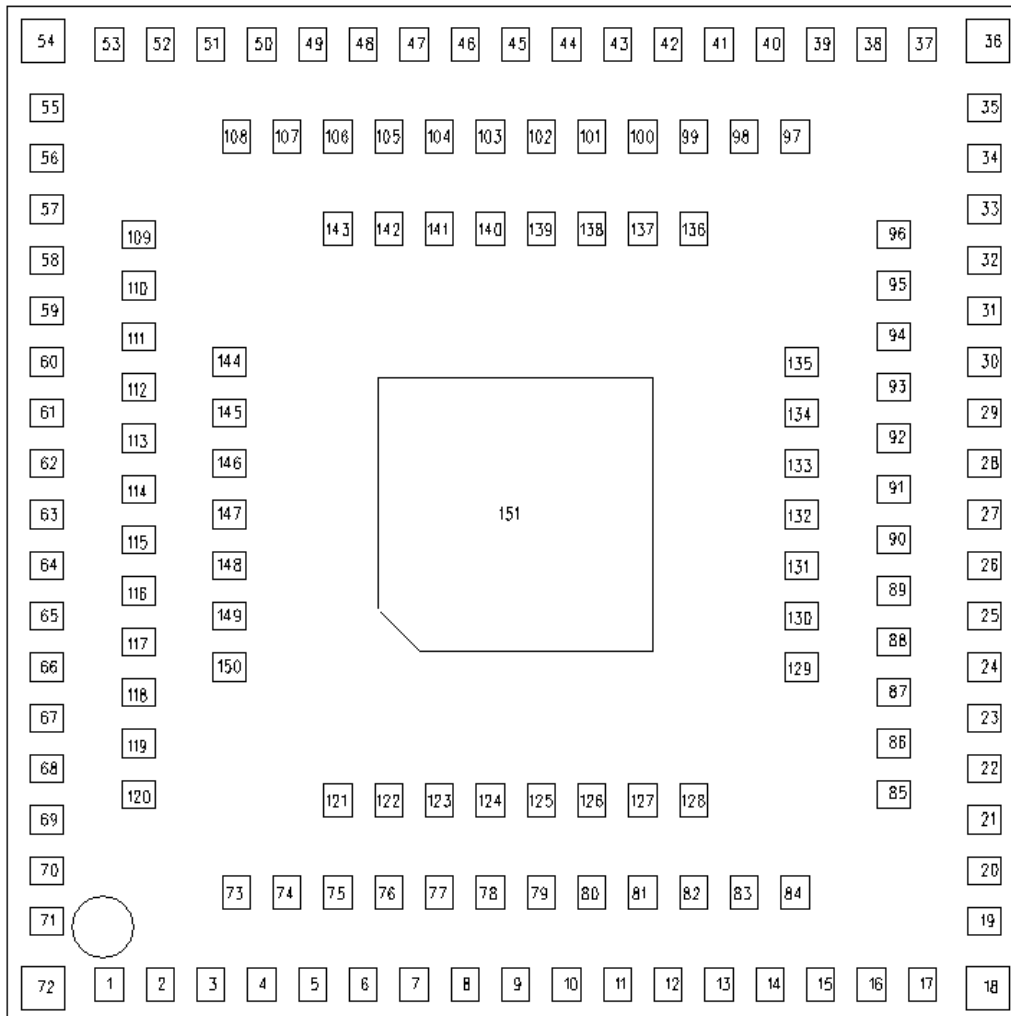


Figure 5: Sterling-EWB base SiP module pinout (top view)

6.2 Base SiP Module Pin Descriptions

Table 1: Sterling-EWB base SiP module pin descriptions

Module Pin	Name	I/O Type	Description	STM32F412 Port
1	ANT	RF	RF TRANSMITTER OUTPUT AND RECEIVE INPUT	
2	GND	GND	GROUND	
3	VDD_3V3_WIFI_PA	PI	WIFI PA POWER SUPPLY	
4	VDD_3V3_WIFI_PA	PI	WIFI PA POWER SUPPLY	
5	GND	GND	GROUND	
6	VDD_3V3_5	PI	DC SUPPLY FOR MCU AND I/O	
7	GND	GND	GROUND	
8	MICRO_SPI1_MOSI	DIO	SPI1_MOSI	PA7
9	QUADSPI_CLK	DIO	QUADSPI_CLK	PB1
10	GND	GND	GROUND	
11	MICRO_SPI4_NSS	DIO	SPI4_NSS	PE11
12	MICRO_SPI4_SCK	DIO	SPI4_SCK	PE12
13	MICRO_SPI4_MISO	DIO	SPI4_MISO	PE13
14	MICRO_SPI4_MOSI	DIO	SPI4_MOSI	PE14
15	GND	GND	GROUND	
16	NC	-	NO CONNECT (DO NOT CONNECT)	
17	NC	-	NO CONNECT (DO NOT CONNECT)	
18	GND	GND	GROUND	
19	NC	-	NO CONNECT (DO NOT CONNECT)	
20	BT_GPIO_3	DIO	WPT_INTb TO WIRELESS CHARGING PMU	
21	MICRO_SPI2_MISO	DIO	SPI2_MISO	PB14
22	MICRO_SPI2_MOSI	DIO	SPI2_MOSI	PB15
23	GND	GND	GROUND	
24	VDD_3V3_3	PI	DC SUPPLY FOR MCU AND I/O	
25	GND	GND	GROUND	
26	NC	-	NO CONNECT (DO NOT CONNECT)	
27	GND	GND	GROUND	
28	VDD3V3_WiFi_IO	PI	DC SUPPLY FOR WIFI AND I/O	
29	GND	GND	GROUND	
30	MICRO_USART1_TX	DO	USART1_TX	PA9
31	MICRO_USART1_RX	DI	USART1_RX	PA10
32	MICRO_USART1_CTS	DI	USART1_CTS	PA11

Module Pin	Name	I/O Type	Description	STM32F412 Port
33	MICRO_USART1_RTS	DO	USART1_RTS	PA12
34	GND	GND	GROUND	
35	MICRO_JTAG_TMS	DI	JTAG_TMS	PA13
36	GND	GND	GROUND	
37	MICRO_JTAG_TCK	DI	JTAG_TCK	PA14
38	MICRO_JTAG_TDI	DI	JTAG_TDI	PA15
39	GND	GND	GROUND	
40	NC	-	NO CONNECT (DO NOT CONNECT)	
41	GND	GND	GROUND	
42	VDD3V3_WIFI	PI	WIFI POWER SUPPLY	
43	VDD3V3_WIFI	PI	WIFI POWER SUPPLY	
44	GND	GND	GROUND	
45	MICRO_JTAG_TDO	DO	JTAG_TDO	PB3
46	MICRO_JTAG_TRSTN	DI	JTAG_TRSTN	PB4
47	GND	GND	GROUND	
48	VDD_3V3_2	PI	DC SUPPLY FOR MCU AND I/O	
49	GND	GND	GROUND	
50	QUADSPI_BK1_IO3	DIO	QUADSPI_BK1_IO3	PF6
51	GND	GND	GROUND	
52	NC	-	NO CONNECT (DO NOT CONNECT)	
53	NC	-	NO CONNECT (DO NOT CONNECT)	
54	GND	GND	GROUND	
55	BT_PCM_CLK	DIO	PCM CLOCK; CAN BE MASTER (OUTPUT) OR SLAVE (INPUT)	
56	NC	-	NO CONNECT (DO NOT CONNECT)	
57	BT_HOST_WAKE	DO	HOST_WAKE	
58	GND	GND	GROUND	
59	VBAT	PI	POWER SUPPLY FOR BACKUP CIRCUIT	
60	GND	GND	GROUND	
61	GND	GND	GROUND	
62	NC	-	NO CONNECT (DO NOT CONNECT)	
63	NC	-	NO CONNECT (DO NOT CONNECT)	
64	GND	GND	GROUND	
65	VDD_3V3	PI	DC SUPPLY FOR MCU AND I/O	

Module Pin	Name	I/O Type	Description	STM32F412 Port
66	GND	GND	GROUND	
67	QUADSPI_BK1_IO1	DIO	QUADSPI_BK1_IO1	PF9
68	QUADSPI_BK1_IO2	DIO	QUADSPI_BK1_IO2	PF7
69	MICRO_I2S2_SD	DIO	I2S2_SD	PC3
70	GND	GND	GROUND	
71	GND	GND	GROUND	
72	GND	GND	GROUND	
73	GND	GND	GROUND	
74	MICRO_SPI1_NSS	DIO	SPI1_NSS	PA4
75	MICRO_SPI1_SCK	DIO	SPI1_SCK	PA5
76	MICRO_SPI1_MISO	DIO	SPI1_MISO	PA6
77	GND	GND	GROUND	
78	QUADSPI_BK2_IO3	DIO	QUADSPI_BK2_IO3	PC5
79	BOOT1/QUADSPI_CLK	DO	BOOT1/QUADSPI_CLK	PB2
80	QUADSPI_BK2_IO0	DIO	QUADSPI_BK2_IO0	PE7
81	QUADSPI_BK2_IO1	DIO	QUADSPI_BK2_IO1	PE8
82	MICRO_I2C2_SCL	DIO	I2C2_SCL	PB10
83	MICRO_I2C2_SDA	DIO	I2C2_SDA	PB11
84	MICRO_SPI2_NSS	DIO	SPI2_NSS	PB12
85	MICRO_SPI2_SCK	DIO	SPI2_SCK	PB13
86	MICRO_GPIO27	DIO	MICRO_GPIO	PD8
87	MICRO_GPIO25	DIO	MICRO_GPIO	PD10
88	NC	-	NO CONNECT (DO NOT CONNECT)	
89	NC	-	NO CONNECT (DO NOT CONNECT)	
90	VDD_USB	PI	DC SUPPLY FOR USB	
91	GND	GND	GROUND	
92	MICRO_I2S2_MCK/MICRO_USART6_TX	DIO	I2S2_MCK/USART6_TX	PC6
93	MICRO_I2S2_CK/MICRO_USART6_RX	DIO	I2S2_CK/USART6_RX	PC7
94	GND	GND	GROUND	
95	NC	-	NO CONNECT (DO NOT CONNECT)	
96	NC	-	NO CONNECT (DO NOT CONNECT)	
97	NC	-	NO CONNECT (DO NOT CONNECT)	
98	NC	-	NO CONNECT (DO NOT CONNECT)	
99	GND	GND	GROUND	

Module Pin	Name	I/O Type	Description	STM32F412 Port
100	NC	-	NO CONNECT (DO NOT CONNECT)	
101	GND	GND	GROUND	
102	MICRO_I2C1_SCL	DIO	I2C1_SCL	PB6
103	MICRO_I2C1_SDA	DIO	I2C1_SDA	PB7
104	BOOT0	DO	BOOT0	BOOT0
105	NC	-	NO CONNECT (DO NOT CONNECT)	
106	MICRO_GPIO0	DIO	MICRO_GPIO	PE3
107	QUADSPI_BK2_NCS	DIO	QUADSPI_BK2_NCS	PC11
108	MICRO_GPIO30	DIO	MICRO_GPIO	PE0
109	NC	-	NO CONNECT (DO NOT CONNECT)	
110	NC	-	NO CONNECT (DO NOT CONNECT)	
111	MICRO_I2S2_DI	DIO	I2S2_DI	PE5
112	GND	GND	GROUND	
113	GND	GND	GROUND	
114	GND	GND	GROUND	
115	GND	GND	GROUND	
116	GND	GND	GROUND	
117	MICRO_RST_N	DI	MICRO_RST_N	NRST
118	QUADSPI_BK1_IO0	DIO	QUADSPI_BK1_IO0	PF8
119	MICRO_WKUP	DI	MICRO_WKUP	PA0
120	GND	GND	GROUND	
121	MICRO_ADC_IN2	DI	ADC_IN2	PA2
122	MICRO_ADC_IN3	DI	ADC_IN3	PA3
123	GND	GND	GROUND	
124	QUADSPI_BK2_IO2	DIO	QUADSPI_BK2_IO2	PC4
125	MICRO_GPIO5	DIO	MICRO_GPIO	PB0
126	RF_SW_CTRL	DIO	ANTENNA DIVERSITY CONTROL	
127	NC	-	NO CONNECT (DO NOT CONNECT)	
128	MICRO_GPIO16	DIO	MICRO_GPIO	PE15
129	BT_GPIO_4	DIO	BSC_SDA TO/FROM WIRELESS CHARGING PMU	
130	BT_GPIO_5	DIO	BSC_SCL FROM WIRELESS CHARGING PMU.	
131	NC	-	NO CONNECT (DO NOT CONNECT)	
132	GND	GND	GROUND	
133	QUADSPI_BK1_NCS	DIO	QUADSPI_BK1_NCS	PG6

Module Pin	Name	I/O Type	Description	STM32F412 Port
134	GND	GND	GROUND	
135	GND	GND	GROUND	
136	NC	-	NO CONNECT (DO NOT CONNECT)	
137	MICRO_GPIO26	DIO	MICRO_GPIO	PD1
138	NC	-	NO CONNECT (DO NOT CONNECT)	
139	NC	-	NO CONNECT (DO NOT CONNECT)	
140	NC	-	NO CONNECT (DO NOT CONNECT)	
141	NC	-	NO CONNECT (DO NOT CONNECT)	
142	MICRO_GPIO28	DIO	MICRO_GPIO	PB8
143	MICRO_I2S2_WS	DIO	I2S2_WS	PB9
144	BT_PCM_SYNC	DIO	PCM SYNC; CAN BE MASTER (OUTPUT) OR SLAVE (INPUT)	
145	BT_PCM_OUT	DO	PCM DATA OUTPUT	
146	BT_PCM_IN	DI	PCM DATA INPUT SENSING	
147	PC13	DIO	MICRO_GPIO	PC13
148	GND	GND	GROUND	
149	GND	GND	GROUND	
150	MICRO_ADC_IN1	DI	ADC_IN1	PA1
151	GND	GND	GROUND	
PI = Power Input		DI = Digital Input		DO = Digital Output
DIO = Bi-directional Digital Port		RF = Bi-directional RF Port		GND = Ground

* If you want to use the USB interface, pins 30-33 (PA9-PA12) can be configured over USART1

7 U.FL/CHIP ANTENNA MODULE FOOTPRINT AND PIN DEFINITIONS

Note: The following footprint and pin definitions apply to the Sterling-EWB U.FL and Chip Antenna variants of the module (453-00013 and 453-00014). There are two module footprints depending on which variant of the module is being used, so it is important to ensure you are using the correct version on your design.

Note on regulatory testing:

It is important that you provide a JTAG interface (same as the DEBUG PROGRAM on the development kit) in your design so that you can load the required regulatory testing software on to your device via the WICED SDK. Please see the EWB Certification Instructions for information on setting up the testing.

7.1 U.FL/Chip Antenna Module Footprint

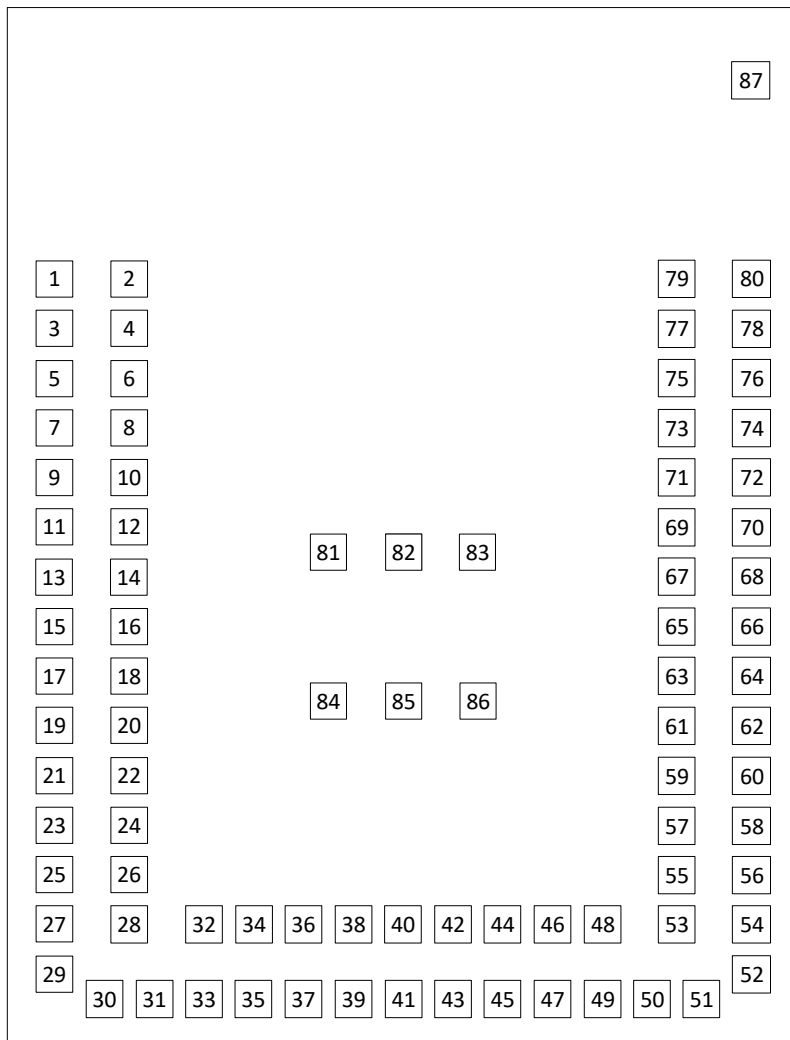


Figure 6: Sterling-EWB U.FL and Chip Antenna module pinout (top view)

7.2 U.FL/Chip Antenna Pin Description

Table 2: Sterling-EWB U.FL and Chip Antenna module pin descriptions

Module Pin	Name	I/O Type	Description
1	GND1	GND	GROUND
2	MICRO_ADC_IN2/PA2	DIO	ADC INPUT OR GENERAL-PURPOSE I/O
3	MICRO_SPI1_SCK/PA5	DIO	SPI SCK OR GENERAL-PURPOSE I/O
4	MICRO_SPI1_NSS/PA4	DIO	SPI NSS OR GENERAL-PURPOSE I/O
5	MICRO_SPI1_MISO/PA6	DIO	SPI MISO OR GENERAL-PURPOSE I/O
6	MICRO_ADC_IN3/PA3	DIO	ADC INPUT OR GENERAL-PURPOSE I/O
7	MICRO_GPIO_5/PB0	DIO	GENERAL-PURPOSE I/O
8	QUADSPI_BK2_IO2/PC4	DIO	QSPI IO2 OR GENERAL-PURPOSE I/O
9	VDD_WIFI_PA	PI	WIFI AND BLUETOOTH POWER SUPPLY
10	GND11	GND	GROUND
11	RF_SW_CNTL	DO	ANTENNA DIVERSITY CONTROL OUTPUT
12	QUADSPI_BK2_IO3/PC5	DIO	QSPI IO3 OR GENERAL-PURPOSE I/O
13	MICRO_SPI1_MOSI/PA7	DIO	SPI MOSI OR GENERAL-PURPOSE I/O
14	BOOT1/QUADSPI_CLK/PB2	DI	BOOT OPTION 1 INPUT
15	QUADSPI_CLK/PB1	DIO	QSPI CLK OR GENERAL-PURPOSE I/O
16	QUADSPI_BK2_IO0/PE7	DIO	QSPI IO0 OR GENERAL-PURPOSE I/O
17	MICRO_SPI4_NSS/PE11	DIO	SPI NSS OR GENERAL-PURPOSE I/O
18	QUADSPI_BK2_IO1/PE8	DIO	QSPI IO1 OR GENERAL-PURPOSE I/O
19	MICRO_SPI4_SCK/PE12	DIO	SPI SCK OR GENERAL-PURPOSE I/O
20	MICRO_I2C2_SCL/PB10	DIO	I2C SCL OR GENERAL-PURPOSE I/O
21	MICRO_SPI4_MISO/PE13	DIO	SPI MISO OR GENERAL-PURPOSE I/O
22	MICRO_I2C2_SDA/PB11	DIO	I2C SDA OR GENERAL-PURPOSE I/O
23	MICRO_SPI4_MOSI/PE14	DIO	SPI MOSI OR GENERAL-PURPOSE I/O
24	MICRO_GPIO_16/PE15	DIO	GENERAL-PURPOSE I/O
25	BT_GPIO_3	DIO	BT GENERAL-PURPOSE I/O
26	MICRO_SPI2_NSS/PB12	DIO	SPI NSS OR GENERAL-PURPOSE I/O
27	MICRO_SPI2_SCK/PB13	DIO	SPI SCK OR GENERAL-PURPOSE I/O
28	MICRO_SPI2_MISO/PB14	DIO	SPI MISO OR GENERAL-PURPOSE I/O
29	GND2	GND	GROUND
30	MICRO_SPI2_MOSI/PB15	DIO	SPI MOSI OR GENERAL-PURPOSE I/O
31	MICRO_GPIO_27/PD8	DIO	GENERAL-PURPOSE I/O

Module Pin	Name	I/O Type	Description
32	MICRO_GPIO_25/PD10	DIO	GENERAL-PURPOSE I/O
33	BT_GPIO_4	DIO	BT GENERAL-PURPOSE I/O
34	BT_GPIO_5	DIO	BT GENERAL-PURPOSE I/O
35	VDD_USB	PI	VUSB POWER SUPPLY
36	QUADSPI_BK1_NCS/PG6	DIO	QSPI NCS OR GENERAL-PURPOSE I/O
37	VDD_MCU	PI	MCU AND IO POWER SUPPLY
38	MICRO_I2S2_CK/MICRO_USART6_RX/PC7	DIO	I2S CK OR USART RX INPUT OR GENERAL-PURPOSE I/O
39	MICRO_I2S2_MCK/MICRO_USART6_TX/PC6	DIO	I2S MCK OR USART TX OUTPUT OR GENERAL-PURPOSE I/O
40	GND12	GND	GROUND
41	VDD_WIFI_IO	PI	WIFI AND BLUETOOTH IO POWER SUPPLY
42	MICRO_USART1_RX/PA10	DI	MCU USART1 RECEIVE INPUT
43	MICRO_USART1_TX/PA9	DO	MCU USART1 TRANSMIT OUTPUT
44	MICRO_GPIO_26/PD1	DIO	GENERAL-PURPOSE I/O
45	MICRO_GPIO_28/PB8	DIO	GENERAL-PURPOSE I/O
46	MICRO_I2C1_SDA/PB7	DIO	I2C SDA OR GENERAL-PURPOSE I/O
47	MICRO_USART1_CTS/PA11	DI	MCU USART1 CLEAR-TO-SEND
48	MICRO_I2C1_SCL/PB6	DIO	I2C SCL OR GENERAL-PURPOSE I/O
49	MICRO_USART1_RTS/PA12	DO	MCU USART1 REQUEST-TO-SEND
50	MICRO_JTAG_TDI	DI	JTAG_TDI
51	MICRO_JTAG_TMS/SWDIO	DI	JTAG_TMS/SWDIO
52	GND3	GND	GROUND
53	BOOT0	DI	BOOT OPTION 0 INPUT
54	MICRO_JTAG_TDO	DI	JTAG_TDO
55	PC13	DIO	GENERAL-PURPOSE I/O
56	MICRO_ADC_IN1/PA1	DIO	ADC INPUT OR GPIO
57	MICRO_JTAG_TCK/SWCLK	DI	JTAG_TCK/SWCLK
58	BT_PCM_IN	DI	PCM DATA INPUT SENSING
59	BT_PCM_OUT	DO	PCM DATA OUTPUT
60	MICRO_RSTN	DI	MCU RESET INPUT
61	BT_PCM_SYNC	DIO	PCM SYNC; CAN BE MASTER (OUTPUT) OR SLAVE (INPUT)
62	VDD_WIFI	PI	WIFI AND BLUETOOTH POWER SUPPLY
63	GND4	GND	GROUND

Module Pin	Name	I/O Type	Description
64	MICRO_JTAG_TRSTN	DI	JTAG_TRSTN
65	MICRO_GPIO_0/PE3	DIO	GENERAL-PURPOSE I/O
66	QUADSPI_BK1_IO0/PF8	DIO	QSPI IO0 OR GENERAL-PURPOSE I/O
67	QUADSPI_BK2_NCS/PC11	DIO	QSPI NCS OR GENERAL-PURPOSE I/O
68	QUADSPI_BK1_IO1/PF9	DIO	QSPI IO1 OR GENERAL-PURPOSE I/O
69	MICRO_I2S2_WS/PB9	DIO	I2S WS OR GENERAL-PURPOSE I/O
70	QUADSPI_BK1_IO3/PF6	DIO	QSPI IO3 OR GENERAL-PURPOSE I/O
71	MICRO_GPIO_30/PE0	DIO	GENERAL-PURPOSE I/O
72	OSC_32K_IN	DI	EXTERNAL SLEEP CLOCK INPUT (not used)
73	MICRO_I2S_DI/PE5	DIO	I2S DATA INPUT OR GENERAL-PURPOSE I/O
74	OSC_32K_OUT	DO	EXTERNAL SLEEP CLOCK INPUT (not used)
75	BT_PCM_CLK	DIO	PCM CLOCK; CAN BE MASTER (OUTPUT) OR SLAVE (INPUT)
76	MICRO_WKUP/PA0	DI	MCU WAKE INPUT
77	BT_HOST_WAKE	DO	HOST_WAKE OR GENERAL-PURPOSE I/O
78	QUADSPI_BK1_IO2/PF7	DIO	QSPI IO2 OR GENERAL-PURPOSE I/O
79	MICRO_I2S2_SD/PC3	DIO	I2S DATA OUTPUT OR GENERAL-PURPOSE I/O
80	VBAT	PI	MCU Battery Backup Power Supply
81	GND5	GND	GROUND
82	GND6	GND	GROUND
83	GND7	GND	GROUND
84	GND8	GND	GROUND
85	GND9	GND	GROUND
86	GND10	GND	GROUND
87	GND13	GND	GROUND

PI = Power Input	DI = Digital Input	DO = Digital Output
DIO = Bi-directional Digital Port	GND = Ground	

8 SPECIFICATIONS

8.1 General Characteristics

Characteristic	Description
Model Name	Sterling-EWB
Product Description	Wi-Fi and Bluetooth wireless module with Cortex™-M4 MCU
SiP Module Dimensions (W x L x T) – mm (in.)	10 x 10 x 1.2 (0.39 x 0.39 x 0.05)
Antenna Option Module Dimensions (W x L x T) – mm (in.)	16 x 21 x 2.8 (0.63 x 0.83 x 0.11)
Operating Temperature – °C (°F)	-40 to +85 (-40 to +185)
Storage Temperature – °C (°F)	-40 to +125 (-40 to +257)
Weight	0.0015167KGS
Moisture Sensitivity Level (MSL)	4
Peak Body Temperature (Peak reflow temperatures during assembly) – °C (°F)	260° (500°F)

8.2 Power Supply Requirements

Power Supply Input	Min	Typical	Max	Unit
VDD_MCU	2.4	3.3	3.6	V
VDD_WIFI	3.0	3.3	3.6	V
VDD_WIFI_IO	3.0	3.3	3.6	V
VDD_WIFI_PA	3.0	3.3	3.6	V
VDD_USB ⁽¹⁾	3.0	3.3	3.6	V
VBAT ⁽²⁾	2.4	3.3	3.6	V

(1) If USB not used, connect VDD_USB input to VDD_MCU

(2) If VBAT not used, connect to VDD_MCU

8.2.1 RF Characteristics

Parameter	Min	Typical	Max	Unit
RF frequency range	2400		2500	MHz
RF data rate	1	802.11 b/g/n rates supported	65	Mbps

8.3 Maximum Ratings

Rating	Value	Unit
VDD_MCU	0 to 4	V
VDD_WIFI	0 to 6	V
VDD_WIFI_IO	0 to 4	V
VDD_WIFI_PA	0 to 6	V
VDD_USB	0 to 4	V
VBAT	0 to 4	V
Voltage ripple any supply input (not to exceed operating voltage)	±2%	Not to exceed operating voltage
Output current sunk by any I/O or control pin	25	mA
Output current sourced by any I/O or control pin	-25	mA
Total output current sunk by sum of all I/O or control pin	120	mA
Total output current sourced by sum of all I/O or control pin	-120	mA

8.4 WLAN Power Consumption

Parameter	Test Conditions	Min	Typical	Max	Unit
11b TX Current	11 Mbps, T _{amb} = +25°C, 3.3V	-	390	-	mA
11g TX Current	54 Mbps, T _{amb} = +25°C, 3.3V	-	310	-	mA
11n TX Current	MCS7, T _{amb} = +25°C, 3.3V	-	290	-	mA
11b RX Current	11 Mbps, T _{amb} = +25°C, 3.3V	-	55	-	mA
11g RX Current	54 Mbps, T _{amb} = +25°C, 3.3V	-	55	-	mA
11n RX Current	MCS7, T _{amb} = +25°C, 3.3V	-	55	-	mA

8.5 Bluetooth Power Consumption

Parameter	Test Conditions	Min	Typical	Max	Unit
EDR TX Current	Constant Transmit, 3DH5, PRBS9 T _{amb} = +25°C, 3.3V	-	50	-	mA
EDR RX Current	Constant Receive, 3DH5 T _{amb} = +25°C, 3.3V	-	30	-	mA
BLE TX Current	T _{amb} = +25°C, 3.3V	-	50	-	mA
BLE RX Current	T _{amb} = +25°C, 3.3V	-	30	-	mA

8.6 WLAN RF Characteristics

8.6.1 WLAN Transmitter Characteristics (TA = +25°C, VCC = 3.3 V)

Parameter	Test Conditions	Min	Typ	Max	Unit
1 Mbps DSSS (b) TX Output Power	1 Mbps BPSK 802.11(b) Mask Compliance 35% EVM RMS power over TX packet	-	17.5	-	dBm
2 Mbps DSSS (b) TX Output Power	2 Mbps QPSK 802.11(b) Mask Compliance 35% EVM RMS power over TX packet	-	17.5	-	dBm
5.5 Mbps DSSS (b) TX Output Power	5.5 Mbps QPSK 802.11(b) Mask Compliance 35% EVM RMS power over TX packet	-	17.5	-	dBm
11 Mbps DSSS (b) TX Output Power	11 Mbps CCK 802.11(b) Mask Compliance 35% EVM RMS power over TX packet	-	17.5	-	dBm
6 Mbps OFDM (g) TX Output Power	6 Mbps BPSK 802.11(g) Mask Compliance -5 dB EVM RMS power over TX packet	-	14.0	-	dBm
9 Mbps OFDM (g) TX Output Power	9 Mbps BPSK 802.11(g) Mask Compliance -8 dB EVM RMS power over TX packet	-	14.0	-	dBm
12 Mbps OFDM (g) TX Output Power	12 Mbps QPSK 802.11(g) Mask Compliance -10 dB EVM RMS power over TX packet	-	14.0	-	dBm
18 Mbps OFDM (g) TX Output Power	18 Mbps QPSK 802.11(g) Mask Compliance -13 dB EVM RMS power over TX packet	-	14.0	-	dBm
24 Mbps OFDM (g) TX Output Power	24 Mbps 16-QAM 802.11(g) Mask Compliance -16 dB EVM RMS power over TX packet	-	14.0	-	dBm
36 Mbps OFDM (g) TX Output Power	36 Mbps 16-QAM 802.11(g) Mask Compliance -19 dB EVM RMS power over TX packet	-	14.0	-	dBm
48 Mbps OFDM (g) TX Output Power	48 Mbps 64-QAM 802.11(g) Mask Compliance -22 dB EVM RMS power over TX packet	-	14.0	-	dBm
54 Mbps OFDM (g) TX Output Power	54 Mbps 64-QAM 802.11(g) Mask Compliance -25 dB EVM RMS power over TX packet	-	14.0	-	dBm
MCS0 OFDM (n) TX Output Power	6.5 Mbps BPSK 802.11(n) Mask Compliance -5 dB EVM RMS power over TX packet	-	12.5	-	dBm
MCS1 OFDM (n) TX Output Power	13 Mbps QPSK 802.11(n) Mask Compliance -10 dB EVM RMS power over TX packet	-	12.5	-	dBm
MCS2 OFDM (n) TX Output Power	19.5 Mbps QPSK 802.11(n) Mask Compliance -13 dB EVM RMS power over TX packet	-	12.5	-	dBm
MCS3 OFDM (n) TX Output Power	26 Mbps 16-QAM 802.11(n) Mask Compliance -16 dB EVM RMS power over TX packet	-	12.5	-	dBm
MCS4 OFDM (n) TX Output Power	39 Mbps 16-QAM 802.11(n) Mask Compliance -19 dB EVM RMS power over TX packet	-	12.5	-	dBm

Parameter	Test Conditions	Min	Typ	Max	Unit
MCS5 OFDM (n) TX Output Power	52 Mbps 64-QAM 802.11(n) Mask Compliance -22 dB EVM RMS power over TX packet	-	12.5	-	dBm
MCS6 OFDM (n) TX Output Power	58.5 Mbps 64-QAM 802.11(n) Mask Compliance -25 dB EVM RMS power over TX packet	-	12.5	-	dBm
MCS7 OFDM (n) TX Output Power	65 Mbps 64-QAM 802.11(n) Mask Compliance -27 dB EVM RMS power over TX packet	-	12.5	-	dBm

8.6.2 WLAN Receiver Characteristics (TA = +25°C, VCC = 3.3 V)

Parameter	Test Conditions	Min	Typ	Max	Unit
1 Mbps DSSS (b) RX Sensitivity	8% PER	-	-93	-	dBm
2 Mbps DSSS (b) RX Sensitivity	8% PER	-	-91	-	dBm
5.5 Mbps DSSS (b) RX Sensitivity	8% PER	-	-89	-	dBm
11 Mbps DSSS (b) RX Sensitivity	8% PER	-	-86	-	dBm
6 Mbps OFDM (g) RX Sensitivity	10% PER	-	-88	-	dBm
9 Mbps OFDM (g) RX Sensitivity	10% PER	-	-87	-	dBm
12 Mbps OFDM (g) RX Sensitivity	10% PER	-	-85	-	dBm
18 Mbps OFDM (g) RX Sensitivity	10% PER	-	-83	-	dBm
24 Mbps OFDM (g) RX Sensitivity	10% PER	-	-80	-	dBm
36 Mbps OFDM (g) RX Sensitivity	10% PER	-	-78	-	dBm
48 Mbps OFDM (g) RX Sensitivity	10% PER	-	-74	-	dBm
54 Mbps OFDM (g) RX Sensitivity	10% PER	-	-72	-	dBm
MCS0 (6.5 Mbps) OFDM (n) RX Sensitivity	10% PER	-	-87	-	dBm
MCS1 (13 Mbps) OFDM (n) RX Sensitivity	10% PER	-	-84	-	dBm
MCS2 (19.5 Mbps) OFDM (n) RX Sensitivity	10% PER	-	-82	-	dBm
MCS3 26 Mbps OFDM (n) RX Sensitivity	10% PER	-	-80	-	dBm
MCS4 39 Mbps OFDM (n) RX Sensitivity	10% PER	-	-77	-	dBm
MCS5 52 Mbps OFDM (n) RX Sensitivity	10% PER	-	-72	-	dBm
MCS6 58.5 Mbps OFDM (n) RX Sensitivity	10% PER	-	-71	-	dBm
MCS7 65 Mbps OFDM (n) RX Sensitivity	10% PER	-	-70	-	dBm

Parameter	Test Conditions	Min	Typ	Max	Unit
11b RX Overload Level	8% PER, 11 Mbps	-10	-	-	dBm
11g RX Overload Level	10% PER, 54 Mbps	-20	-	-	dBm
11n RX Overload Level	10% PER, MCS7	-20	-	-	dBm

8.7 Bluetooth RF Characteristics

8.7.1 Bluetooth Transmitter GFSK & EDR Characteristics (TA=25°C, VDD=3.3 V)

Parameter	Test Conditions	Min	Typical	Max	Bluetooth Spec	Unit
GFSK RF Output Power		-	8.5	-		dBm
EDR RF Output Power		-	4.0	-		dBm
Power Control Step Size		2	4	8	2-8	dB
EDR Relative Power		-4		1	-4/+1	dB

8.7.2 Bluetooth Receiver GFSK & EDR Characteristics (TA=25°C, VDD=3.3 V)

Table 3: Bluetooth receiver RF characteristics

Parameter	Test Conditions	Min	Typical	Max	Bluetooth Spec	Unit
GFSK Sensitivity	BER=0.1%	-	-90	-	-70	dBm
EDR 2 Mbps Sensitivity	BER=0.01%	-	-92	-	-70	dBm
EDR 3 Mbps Sensitivity	BER=0.01%	-	-87	-	-70	dBm
GFSK Maximum Input Level	BER=0.1%	-	-20	-	-20	dBm
EDR 2 Maximum Input Level	BER=0.01%	-	-20	-	-	dBm
EDR 3 Maximum Input Level	BER=0.01%	-	-20	-	-	dBm

8.7.3 BLE Transmitter Characteristics (TA=25°C, VDD=3.3 V)

Table 4: BLE transmitter RF characteristics

Parameter	Test Conditions	Min	Typical	Max	Bluetooth Spec	Unit
GFSK RF Output Power		-	7.5	-		dBm
Power Control Step Size		2	4	8	2-8	dB

8.7.4 BLE Receiver Characteristics (TA=25°C, VDD=3.3 V)

Table 5: BLE receiver RF characteristics

Parameter	Test Conditions	Min	Typical	Max	Bluetooth Spec	Unit
GFSK Sensitivity	PER = 30.8%	-	-94	-	-70	dBm
GMSK Maximum Input Level	PER = 30.8%	-	-20	-	-20	dBm

9 MCU INTERFACE CHARACTERISTICS

9.1 DC Characteristics – General Input and Output

Table 6: DC characteristics MCU I/O

Parameter	Test Conditions	Min	Max	Unit
Logic input low, V_{IL}	$2.4V \leq VDD_MCU \leq 3.6V$	-	$0.3V_{DD}$	V
Logic input high, V_{IH}	$2.4V \leq VDD_MCU \leq 3.6V$	$0.7V_{DD}$	-	V
BOOT0 Logic input low, V_{IL}	$2.4V \leq VDD_MCU \leq 3.6V$	-	$0.1V_{DD} + 0.1$	V
BOOT0 Logic input high, V_{IH}	$2.4V \leq VDD_MCU \leq 3.6V$	$0.17V_{DD} + 0.7$	-	V
Logic output low, V_{OL}	$2.7V \leq VDD_MCU \leq 3.6V$ CMOS port, $I_{IO} = +8mA$	-	0.4	V
	$2.7V \leq VDD_MCU \leq 3.6V$ TTL port, $I_{IO} = +8mA$	-	0.4	
	$2.7V \leq VDD_MCU \leq 3.6V$ $I_{IO} = +20mA$	-	1.3	
	$2.4V \leq VDD_MCU \leq 3.6V$ $I_{IO} = +6mA$	-	0.4	
	$2.4V \leq VDD_MCU \leq 3.6V$ $I_{IO} = +4mA$	-	0.4	
Logic output high, V_{OH}	$2.7V \leq VDD_MCU \leq 3.6V$ CMOS port, $I_{IO} = +8mA$	$V_{DD} - 0.4$	-	V
	$2.7V \leq VDD_MCU \leq 3.6V$ TTL port, $I_{IO} = +8mA$	2.4	-	
	$2.7V \leq VDD_MCU \leq 3.6V$ $I_{IO} = +20mA$	$V_{DD} - 1.3$	-	
	$2.4V \leq VDD_MCU \leq 3.6V$ $I_{IO} = +6mA$	$V_{DD} - 0.4$	-	
	$2.4V \leq VDD_MCU \leq 3.6V$ $I_{IO} = +4mA$	$V_{DD} - 0.4$	-	

TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52

9.2 I2C Interface

9.2.1 Overview

The Sterling-EWB Module MCU section supports Standard and Fast mode I2C communication.

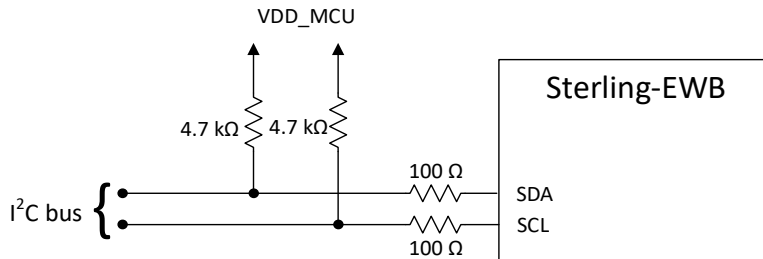
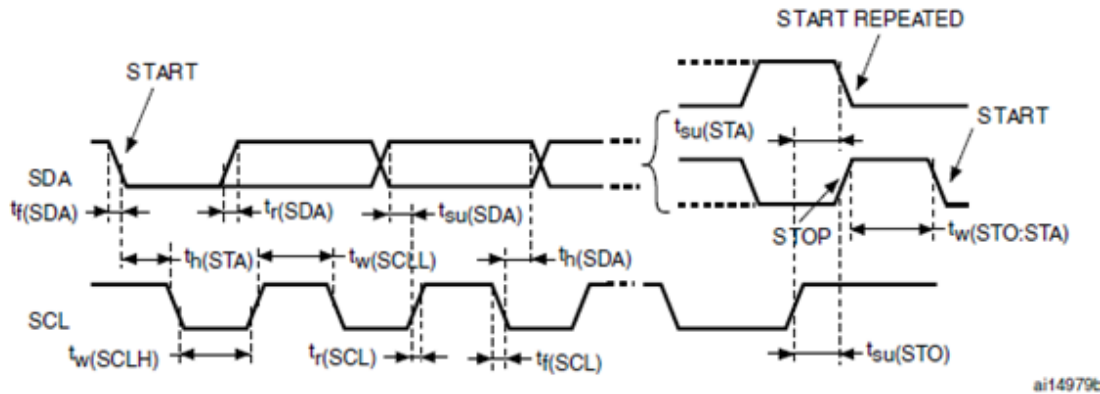


Table 7: Signal connections to I2C bus

Symbol	Parameter	Standard Mode ⁽¹⁾		Fast Mode ⁽¹⁾⁽²⁾		Unit
		Min	Max	Min	Max	
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	μs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	μs
$t_{su(SDA)}$	SDA setup time	250	-	100	-	ns
$t_h(SDA)$	SDA data hold time	0	3450 ⁽³⁾	0	900 ⁽⁴⁾	ns
$t_r(SDA)$ $t_r(SCL)$	SDA and SCL rise time	-	1000	-	300	ns
$t_f(SDA)$ $t_f(SCL)$	SDA and SCL fall time	-	300	-	300	ns
$t_h(SDA)$	Start condition hold time	4.0	-	0.6	-	μs
$t_{su(STA)}$	Repeated Start condition setup time	4.7	-	0.6	-	μs
$t_{su(STO)}$	Stop condition setup time	4.0	-	0.6	-	μs
$t_{sw(STO:STA)}$	Stop to Start condition time (bus free)	4.7	-	1.3	-	μs
t_{SP}	Pulse width of the spikes that are suppressed by the analog filter for standard fast mode	0	50	0	50	μs
C_b	Capacitive load for each bus line	-	400	-	400	pF

1. Guaranteed by design, not tested in production.
2. f_{PCLK1} must be at least 2 MHz to achieve standard mode I2C frequencies. It must be at least 4MHz to achieve fast mode I2C frequencies, and a multiple of 10MHz to reach the 400 kHz maximum I2C fast mode clock.
3. The device must internally provide a hold time of at least 300ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.

4. The maximum data hold time has only to be met if the interface does not stretch the low period of SCL signal.



Measurement points are done at 0.3V_{DD} and 0.7V_{DD}

9.3 SPI Interface

Table 8: SPI interface characteristics

Parameter	Test Conditions	Min	Typical	Max	Unit
SPI Clock Frequency	Master full duplex/receiver mode 2.7V < VDD_MCU < 3.6V SPI1/4/5	-	-	42	MHz
	Master full duplex/receiver mode 3.0V < VDD_MCU < 3.6V SPI1/4/5	-	-	50	
	Master transmitter mode 2.4V < VDD_MCU < 3.6V SPI1/4/5	-	-	50	
	Master mode 2.4V < VDD_MCU < 3.6V SPI1/2/3/4/5	-	-	25	
	Slave transmitter/full duplex mode 2.7V < VDD_MCU < 3.6V SPI1/4/5	-	-	38 ⁽¹⁾	
	Slave receiver mode 2.4V < VDD_MCU < 3.6V SPI1/4/5	-	-	50	
Duty cycle of SPI Clock	Slave mode	30	50	70	%
	Slave mode	30	50	70	%
SCK high and low time	Master mode, SPI presc = 2	T _{PCLK} - 1.5	T _{PCLK}	T _{PCLK} - 1.5	ns
NSS setup time	Slave mode, SPI presc = 2	3T _{PCLK}	-	-	ns
NSS hold time	Slave mode, SPI presc = 2	2T _{PCLK}	-	-	ns
Data input setup time	Master mode	4	-	-	ns
	Slave mode	2.5	-	-	ns
Data input hold time	Master mode	7.5	-	-	ns
	Slave mode	3.5	-	-	ns

10 MCU UART INTERFACES

10.1 Overview

The Sterling-EWB is configurable for up to three UART interfaces for serial communications. The UART is a standard 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 9600 bps to 4.0 Mbps. The interface features an automatic baud rate detection capability that returns a baud rate selection. The baud rate may also be selected through a vendor-specific UART HCI command.

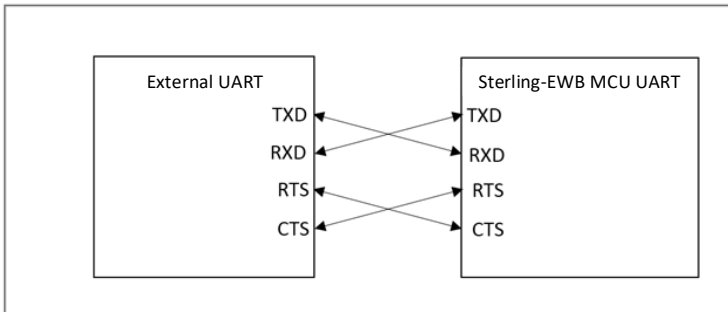


Figure 7: UART connection between Sterling-EWB and external device

10.2 Soldering Recommendations

10.2.1 Reflow for Lead Free Solder Paste

- Optimal solder reflow profile depends on solder paste properties and should be optimized as part of an overall process development.
- It is important to provide a solder reflow profile that matches the solder paste supplier's recommendations.
- Temperature ranges beyond that of the solder paste supplier's recommendation could result in poor solderability.
- All solder paste suppliers recommend an ideal reflow profile to give the best solderability.

10.3 Recommended Reflow Profile for Lead Free Solder

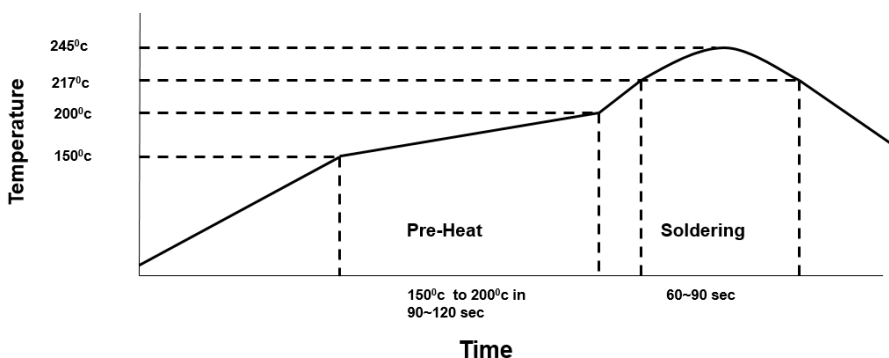


Figure 8: Recommended soldering profile

Note: The quality of solder joints on the surface mount pads where they contact the host board should meet the appropriate IPC Specification. See *IPC-A-610-D Acceptability of Electronic Assemblies*, section 8.2.1 *Bottom Only Terminations*.

Peak body temperature (peak reflow temperatures during assembly): 260° (500°F)

11 Wi-Fi MAC IDs/BLUETOOTH MAC IDs

Table 9: Example of MAC ID assignments

	Wi-Fi MAC ID	Bluetooth MAC ID
Module 1	C0:EE:40:07:00:01	C0:EE:40:07:00:02
Module 2	C0:EE:40:07:00:03	C0:EE:40:07:00:04
Module 3	C0:EE:40:07:00:05	C0:EE:40:07:00:06
Module 4	C0:EE:40:07:00:07	C0:EE:40:07:00:08

12 MECHANICAL DETAILS

12.1 Base SiP Module Mechanical Data

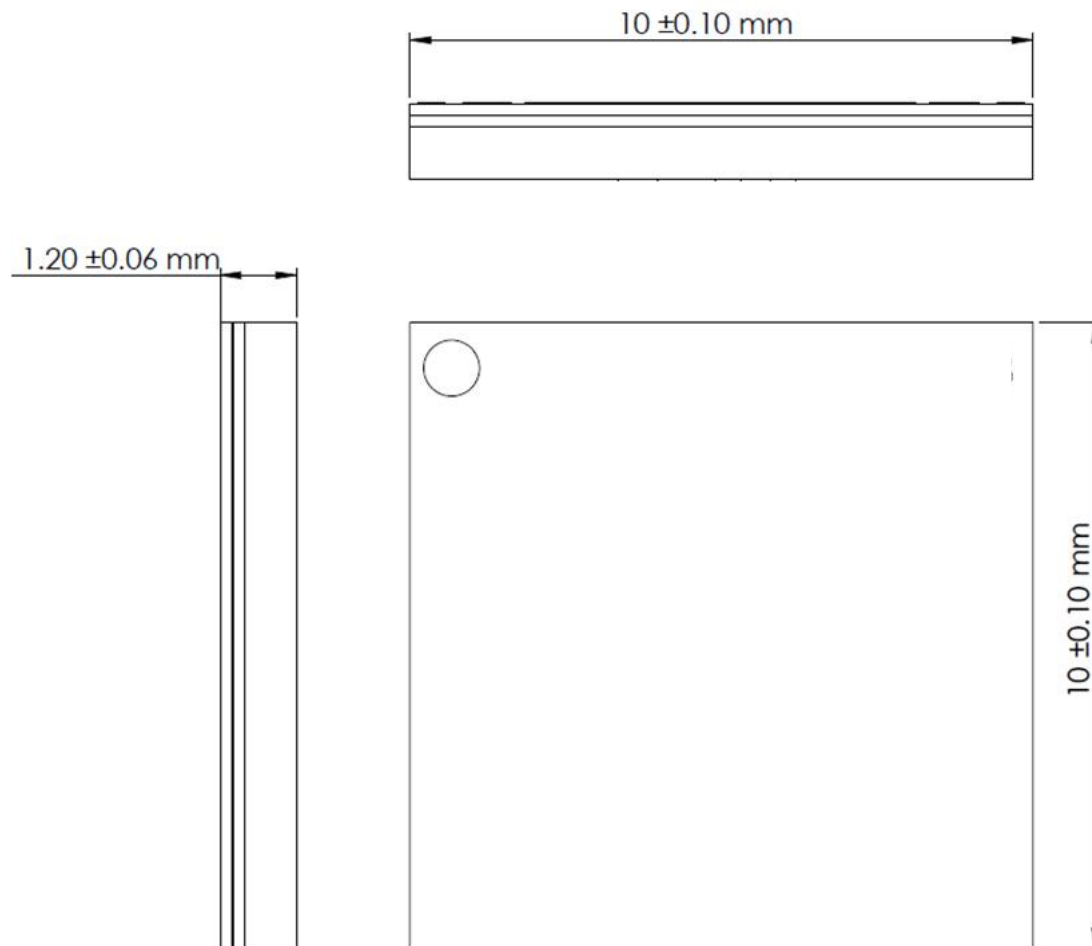


Figure 9: Base SiP module mechanical dimensions

12.3 Base SiP Module Recommended Solder Stencil

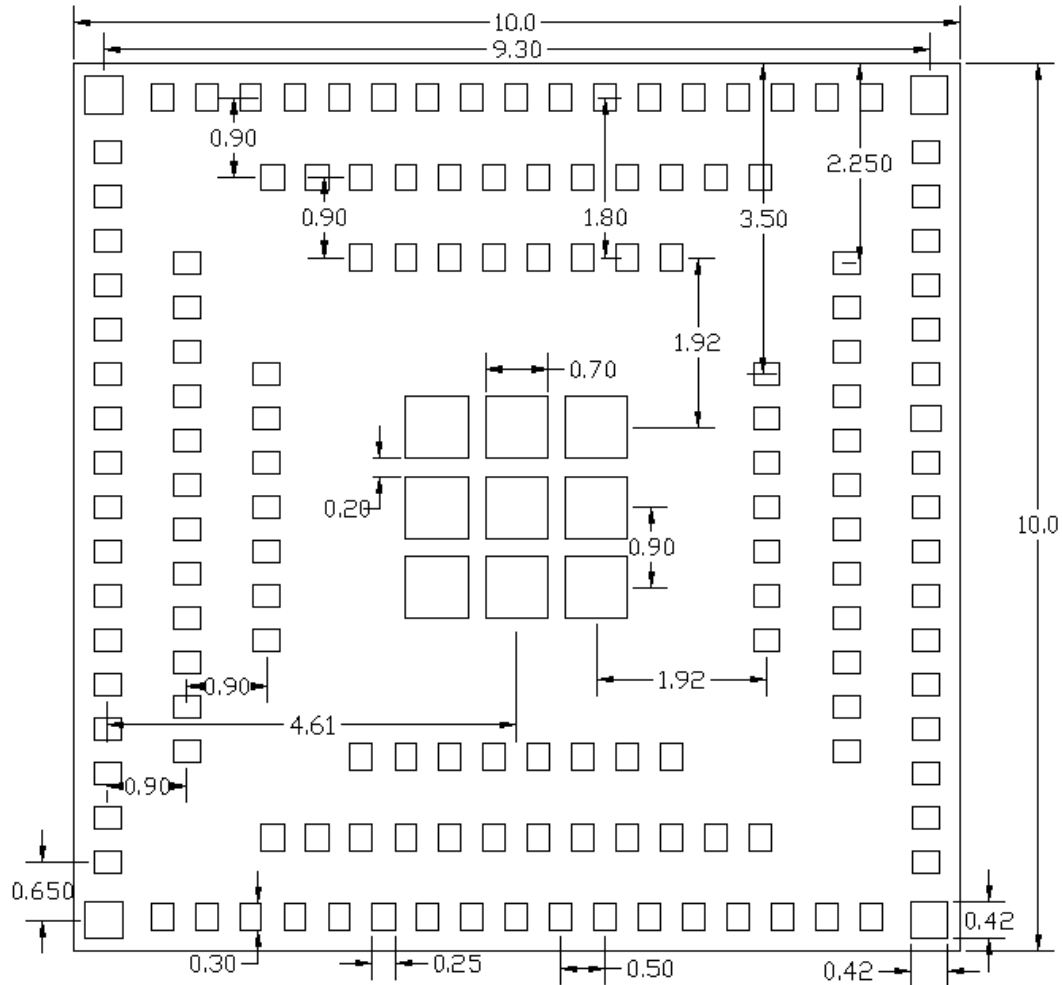


Figure 11: Base SiP module recommended solder stencil (top view)

Note: Solder mask and paste mask to be adjusted according to end-user's assembly process.

12.4 Base SiP Module Tape and Reel Packaging

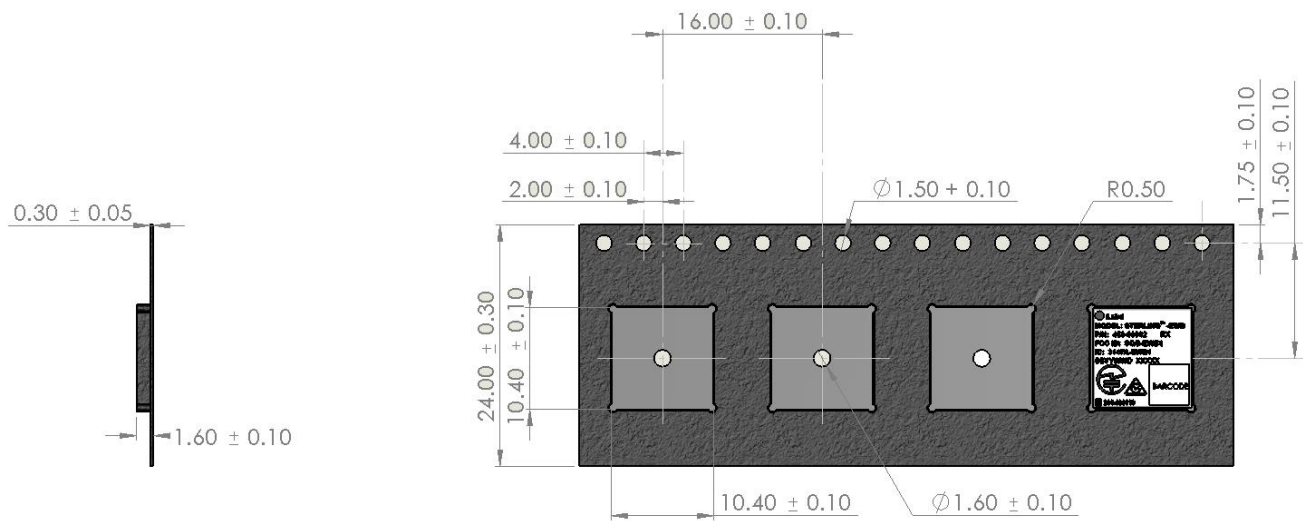


Figure 12: Base SiP module tape and reel specification

Notes:

- 1) DIM in mm
- 2) 10 sprocket hole pitch cumulative tolerance ± 0.10 mm
- 3) Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole
- 4) Full reel contains 2000 modules

The module must be in this orientation when feeding the tape.

12.6 U.FL and Chip Antenna Tape and Reel Packaging

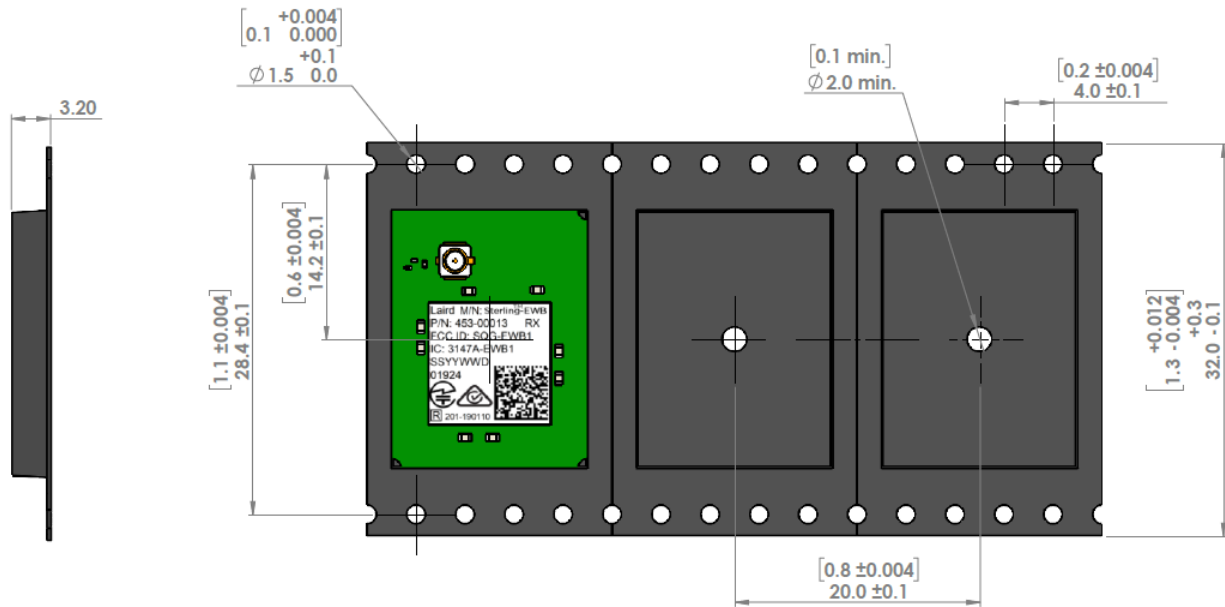
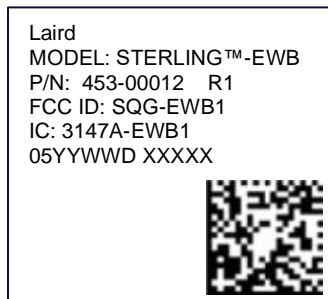


Figure 14: U.FL and chip antenna modules tape and reel specification (full reel contains 1000 modules)

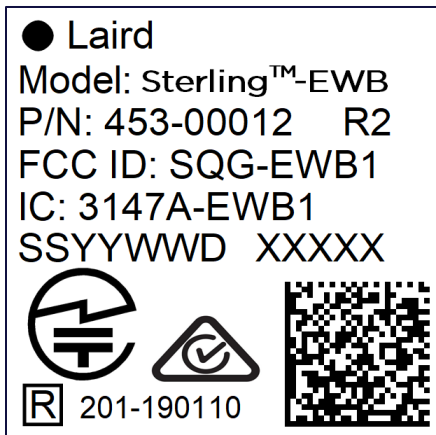
12.7 Device Markings

12.7.1 SiP Module

The shield on the 453-00012 base module contains the following information:

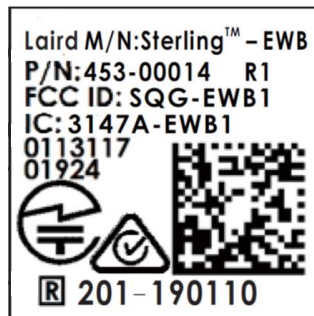


Latest Version:



12.7.2 Antenna Option Modules

The shield on the 453-00013 and 453-00014 modules contains the following information:



13 CLEANING

In general, cleaning the populated modules is strongly discouraged. Residuals under the module cannot be easily removed with any cleaning process.

- Cleaning with water can lead to capillary effects where water is absorbed into the gap between the host board and the module. The combination of soldering flux residuals and encapsulated water could lead to short circuits between neighboring pads. Water could also damage any stickers or labels.
- Cleaning with alcohol or a similar organic solvent will likely flood soldering flux residuals into the RF shield, which is not accessible for post-washing inspection. The solvent could also damage any stickers or labels.
- Ultrasonic cleaning could damage the module permanently.

14 OPTICAL INSPECTION

After soldering the module to the host board, consider optical inspection to check the following:

- Proper alignment and centering of the module over the pads.
- Proper solder joints on all pads.
- Excessive solder or contacts to neighboring pads, or vias.

15 REWORK

The Sterling-EWB module can be unsoldered from the host board if the Moisture Sensitivity Level (MSL) requirements are met as described in this datasheet.

Note: Never attempt a rework on the module itself, e.g. replacing individual components. Such actions will terminate warranty coverage.

16 SHIPPING, HANDLING, AND STORAGE

16.1 Shipping

Bulk orders of the Sterling-EWB base module are delivered in reels of 2000. Bulk orders for the antenna option PCBAs are delivered in reels of 1000.

16.2 Handling

The Sterling-EWB modules contain a highly sensitive electronic circuitry. Handling without proper ESD protection may damage the module permanently.

16.3 Moisture Sensitivity Level (MSL)

Per J-STD-020, devices rated as MSL 4 and not stored in a sealed bag with desiccant pack should be baked prior to use.

Devices are packaged in a Moisture Barrier Bag with a desiccant pack and Humidity Indicator Card (HIC). Devices that will be subjected to reflow should reference the HIC and J-STD-033 to determine if baking is required.

If baking is required, refer to J-STD-033 for bake procedure.

Sterling-EWB MSL level: Level 4

16.4 Storage

Per J-STD-033, the shelf life of devices in a Moisture Barrier Bag is 12 months at <40C and <90% room humidity (RH).

Do not store in salty air or in an environment with a high concentration of corrosive gas, such as Cl₂, H₂S, NH₃, SO₂, or NO_x.

Do not store in direct sunlight.

The product should not be subject to excessive mechanical shock.

16.5 Repeated Reflow Soldering

Only a single reflow soldering process is encouraged for host boards.

Peak body temperature (peak reflow temperatures during assembly): 260° (500°F)

17 REGULATORY

Note: For complete regulatory information, refer to the [Sterling-EWB Regulatory Information](#) document which is also available from the [Sterling-EWB product page](#).

The Sterling-EWB holds current certifications in the following countries:

Model	US/FCC	Canada/ISED	Japan/MIC
Sterling-EWB	SQG-EWB1	3147A-EWB1	201-190110

Note on regulatory testing:

It is important that you provide a JTAG interface (same as the DEBUG PROGRAM on the development kit) in your design so that you can load the required regulatory testing software on to your device via the WICED SDK. Please see the EWB Certification Instructions for information on setting up the testing.

18 BLUETOOTH SIG QUALIFICATION

18.1 Overview

The Sterling-EWB module is listed on the Bluetooth SIG website as a qualified Controller Subsystem.

Table 10: Sterling-EWB declaration ID

Design Name	Owner	Declaration ID	Design Description
453-00013C	Laird	D043845	Sterling-EWB U.FL module (Cut Tape)
453-00013R	Laird	D043845	Sterling-EWB U.FL module (Tape and Reel)
453-00014C	Laird	D043845	Sterling-EWB chip antenna module (Cut Tape)
453-00014R	Laird	D043845	Sterling-EWB chip antenna module (Tape and Reel)
453-00012C	Laird	D043845	Sterling-EWB base SiP module (Cut Tape)
453-00012R	Laird	D043845	Sterling-EWB base SiP module (Tape and Reel)

It is a mandatory requirement of the Bluetooth Special Interest Group (SIG) that every product implementing Bluetooth technology has a Declaration ID. Every Bluetooth design is required to go through the qualification process, even when referencing a Bluetooth Design that already has its own Declaration ID. The Qualification Process requires each company to register as a member of the Bluetooth SIG – www.bluetooth.com

The following is a link to the Bluetooth Registration page: <https://www.bluetooth.com/develop-with-bluetooth/join/>

For each Bluetooth Design it is necessary to purchase a Declaration ID. This can be done before starting the new qualification, either through invoicing or credit card payment. The fees for the Declaration ID will depend on your membership status, please refer to the following webpage:

<https://www.bluetooth.com/develop-with-bluetooth/qualification-listing/qualification-listing-fees/>

A Declaration ID can be purchased via the following link:

<https://launchstudio.bluetooth.com/MyProjects/ManageDeclarationIds>

18.2 Qualification Steps When Referencing a Laird Controller Subsystem Design

To qualify your product when referencing a Laird Controller Subsystem design, follow these steps:

1. To start a listing, go to: <https://launchstudio.bluetooth.com/MyProjects/GettingStarted>

Note: A username and password are required to access this site.

2. Select the option, 'Start the Bluetooth Qualification Process with **No Required Testing**'.
3. Enter your Project Name and then enter **136198** in Referenced Qualified Design.
4. Repeat this step for all Subsystems used in your design, (this may be just a Host Subsystem or in addition a Profile Subsystem). You will need to add the QDID for each Subsystem referenced in your design.

Note: If there is no associated Host Subsystem then it will be necessary to list your own Host Subsystem, this would be possible by following option, 'Start the Bluetooth Qualification Process with Required Testing'. In this case you will add a Host Component Design in the 'Referenced Qualified Design' drop down. An example of this is the Cypress CY-WICED 4.0 Bluetooth Host Software Stack, QDID 115853. It will be necessary to follow the more complex route for this listing. Once your Host Subsystem listing is complete, you would simply reference the Sterling LWB Design in the final listing steps, using QDID 136198. Contact your Laird representative for assistance, contact details are at the bottom of this document.

5. When all referenced Subsystems have been entered, hit 'Save and continue to Product Declaration'.
6. Enter your preferred listing date, (note it's possible to delay the public listing date up to 90 days).
7. The next step is to add all Products that contain the Subsystem combination as declared in step 3 and 4. Additional products can be added at a later date if required, as long as they use the same subsystem combination. Each product should have its own entry, to add a similar product use the 'Duplicate' button and edit as required.
8. Once all products are added, hit 'Save and continue to Declaration ID', if you have already purchased an ID select the correct one from the listed IDs or hit 'Purchase Declaration ID page'.

Note: Unless the Declaration ID is pre-paid or purchased with a credit card, you cannot proceed until the SIG invoice is paid.

9. Once the Declaration ID is selected, tap **Save and continue to Review**. The Project Status items should all be ticked in green, then check all details are correct, go back and amend if required. You should now read and select all statements, add your name to the Signature box, and tap **Signature Confirmed – Complete Project & Submit Product(s) for Qualification**.

Your new design will be listed on the SIG website and you can download a copy of your SDoC. You can also check your listing by hitting 'View Listing Details'.

For further information please refer to the following training material:

<https://www.bluetooth.com/wp-content/uploads/2019/04/Launch-Studio-Checklist.pdf>

18.3 Additional Assistance

Please contact your local sales representative or our support team for further assistance:

Email support@lairdconnect.com

Phone Americas: +1-800-492-2320
Europe: +44-1628-858-940
Hong Kong: +852 2923 0610

Web <https://www.lairdconnect.com/wireless-modules>